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10/826,668	04/16/2004	Jack C. Wybenga	2003.09.008.BN0	9601

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/826,668	WYBENGA ET AL.	
	Examiner	Art Unit	
	Robert C. Scheibel	2619	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims **1, 10, and 19** are objected to because of the following informalities:

The phrase "capable of" in these claims (four instances in claims 1 and 10 and one instance in claim 19) do not positively recite the limitation(s) which follow this phrase; as such, the claim language suggests or makes optional this limitation, but does not require it. (See MPEP section 2111.04 for more information.) Further, it has been held that the recitation that an element is "capable of" perform a function is not a positive limitation but only requires the ability to so perform. It does not constitute a limitation in any patentable sense. In re Hutchison, 69 USPQ 138. Appropriate correction is required. This language should be amended to positively recite these limitations. For example, the phrase "packet processing circuitry capable of transmitting data packets..." in lines 5-6 of claim 1 should be amended to "packet processing circuitry that transmits data packets..." or the like. Without an amendment such as this to the language, nearly any communications circuitry will read on this limitation as nearly any communications circuitry is ***capable of*** transmitting data packets (whether or not the art specifically indicates that the circuitry exchanges packets).

Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims **1-23** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

4. Claims **1 and 10** recite the limitation "said data packets" in lines 14 and 18 of claim 1 and lines 15 and 19 of claim 10. There is insufficient antecedent basis for this limitation in the claim; it is unclear to which of the data packets recited earlier in the claims this phrase refers.

5. Claims **2-5 and 11-14** recite the limitation "said security and classification functions" in lines 1-2 of claims 2-5 and line 2 of claims 11-14. There is insufficient antecedent basis for this limitation in the claim; it is unclear to which of the security and classification functions recited earlier in the claims this phrase refers.

6. Claims **19-23** recite the limitation "the security and classification functions" in line 15 of claim 19 and lines 1-2 of claims 20-23. There is insufficient antecedent basis for this limitation in the claim; it is unclear to which of the security and classification functions recited earlier in the claims this phrase refers.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

9. Claims **1, 6-10, and 15-19** are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent Application Publication 20030231625 to Calvignac et al in view of U.S. Patent 6,393,026 to Irwin.

Regarding claims **1 and 10**, Calvignac discloses a router for interconnecting external devices coupled to said router, said router comprising:

a switch fabric (switch fabric 60 of Figure 2 and the switch fabric not shown in Figure 4A which connects to the switch interfaces (see paragraph 37 on page 4)); and

a plurality of routing nodes coupled to said switch fabric (router blades 80, 90, and 100 of Figure 2; note that element 150 of Figure 4A is also a router blade), wherein each of said plurality of routing nodes comprises packet processing circuitry capable of transmitting data packets to, and receiving data packets from, said external devices (the router blade transmits data to/from the network media via ports 152 and 154) and further capable of transmitting data packets to, and receiving data packets from, other ones of said plurality of routing nodes via said switch fabric (similarly, the router blade transmits data to/from the switch fabric via switch interface 156 and 158), wherein said packet processing circuitry comprises:

a first network processor (the ingress portion of the router blade shown in Figure 4B; this can be implemented as a single chip/processor as indicated in the last sentence of paragraph 3 on page 1) capable of performing security and classification functions associated with said data packets (see the description of the classification and security (firewall) functions throughout; consider paragraphs 5 on page 1 and 47 on page 5); and

a second network processor (the egress portion of the router blade (analogous to the ingress portion shown in Figure 4B); this can be implemented as a single chip/processor as indicated in the last sentence of paragraph 3 on page 1) capable of performing security and classification functions associated with said data packets (see the description of the classification and security (firewall) functions throughout; consider paragraphs 5 on page 1 and 47 on page 5).

Further regarding claim **10**, Calvignac discloses the communication network in Figure 1.

Similarly regarding claim **19**, Calvignac discloses the method limitations which are analogous to the claim 1 limitations as above.

Calvignac does not disclose expressly the limitations that the first and second network processor is implemented using a plurality of microengines. However, Irwin clearly discloses a router blade (called a forwarding engine 18 in Irwin) is implemented using a multiprocessor architecture. Specifically, the computing nodes 110 of Figure 7 of Irwin disclose the microengines of the independent claims.

Calvignac and Irwin are analogous art because they are from the same field of endeavor of high-speed data routing. At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement the ingress circuitry of Figure 4B of Calvignac with the multiprocessor architecture of Figure 7 of Irwin. Similarly, it would have been obvious to

replace the analogous egress circuitry of Calvignac with the multiprocessor architecture of Figure 7 of Irwin. The motivation for doing so would have been to achieve high processor utilization and provide algorithmic flexibility as suggested by Irwin in lines 45-50 of column 3. In fact, Irwin discloses as the prior art upon which his solution improves, an architecture which is very similar at a high level to the solution of Calvignac. Calvignac can be characterized as analogous to either the implementation using a single processor (Figure 1) or the implementation using multiple processors each carrying out separate functionality (Figure 3). Throughout the document, Irwin demonstrates how the architecture of Figure 7, for example, improves on an architecture similar to that of Calvignac.

Therefore, it would have been obvious to combine Irwin with Calvignac for the benefit of higher processor utilization and algorithmic flexibility to obtain the invention as specified in claims 1, 10, and 19.

Regarding claims **6 and 15**, the above combination of Calvignac and Irwin discloses the limitations of parent claims 1 and 10. Calvignac does not expressly disclose the limitations of claims 6 and 15 that a first one of said first plurality of microengines is capable of executing N threads, wherein each of said N threads performs at least one security and classification function.

However, Irwin discloses the limitations of claims 6 and 15 that a first one of said first plurality of microengines is capable of executing N threads, wherein each of said N threads performs at least one security and classification function (see lines 6-23 of column 7; clearly a plurality of threads runs on the multiprocessors of Irwin, and the software procedures represent the at least one security and classification function of the claim). This multithreaded behavior of

Irwin is a key part of the multiprocessor implementation discussed relative to claims 1 and 10 above.

Calvignac and Irwin are analogous art because they are from the same field of endeavor of high-speed data routing. At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement the ingress circuitry of Figure 4B of Calvignac with the multiprocessor architecture of Figure 7 of Irwin as above for claims 1 and 10. Similarly, it would have been obvious to replace the analogous egress circuitry of Calvignac with the multiprocessor architecture of Figure 7 of Irwin. Furthermore, it would have been obvious to a person of ordinary skill in the art to implement the multiprocessor architecture of Irwin using the multithreaded approach discussed above. The motivation for doing so would have been to achieve high processor utilization and provide algorithmic flexibility as suggested by Irwin in lines 45-50 of column 3. In fact, Irwin discloses as the prior art upon which his solution improves, an architecture which is very similar at a high level to the solution of Calvignac. Calvignac can be characterized as analogous to either the implementation using a single processor (Figure 1) or the implementation using multiple processors each carrying out separate functionality (Figure 3). Throughout the document, Irwin demonstrates how the architecture of Figure 7, for example, improves on an architecture similar to that of Calvignac.

Therefore, it would have been obvious to combine Irwin with Calvignac for the benefit of higher processor utilization and algorithmic flexibility to obtain the invention as specified in claims 6 and 15.

Regarding claims 7 **and 16**, the above combination of Calvignac and Irwin discloses the limitations of parent claims 6 and 15. Calvignac does not expressly disclose the limitations of

claims 7 and 16 that a first one of said second plurality of microengines is capable of executing M threads, wherein each of said M threads performs at least one security and classification function.

However, Irwin discloses the limitations of claims 7 and 16 that a first one of said second plurality of microengines is capable of executing M threads, wherein each of said M threads performs at least one security and classification function (see lines 6-23 of column 7; clearly a plurality of threads runs on the multiprocessors of Irwin, and the software procedures represent the at least one security and classification function of the claim). This multithreaded behavior of Irwin is a key part of the multiprocessor implementation discussed relative to claims 1 and 10 above.

Calvignac and Irwin are analogous art because they are from the same field of endeavor of high-speed data routing. At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement the ingress circuitry of Figure 4B of Calvignac with the multiprocessor architecture of Figure 7 of Irwin as above for claims 1 and 10. Similarly, it would have been obvious to replace the analogous egress circuitry of Calvignac with the multiprocessor architecture of Figure 7 of Irwin. Furthermore, it would have been obvious to a person of ordinary skill in the art to implement the multiprocessor architecture of Irwin using the multithreaded approach discussed above. The motivation for doing so would have been to achieve high processor utilization and provide algorithmic flexibility as suggested by Irwin in lines 45-50 of column 3. In fact, Irwin discloses as the prior art upon which his solution improves, an architecture which is very similar at a high level to the solution of Calvignac. Calvignac can be characterized as analogous to either the implementation using a single

processor (Figure 1) or the implementation using multiple processors each carrying out separate functionality (Figure 3). Throughout the document, Irwin demonstrates how the architecture of Figure 7, for example, improves on an architecture similar to that of Calvignac.

Therefore, it would have been obvious to combine Irwin with Calvignac for the benefit of higher processor utilization and algorithmic flexibility to obtain the invention as specified in claims 7 and 16.

Regarding claims **8 and 17**, Calvignac discloses the limitation that said first network processor processes data packets being transmitted from said external devices to said switch fabric (the ingress circuitry of Figure 4B).

Regarding claims **9 and 18**, Calvignac discloses the limitation that said second network processor processes data packets being transmitted from said switch fabric to said external devices (the egress circuitry analogous to the ingress circuitry of Figure 4B).

10. Claims **2, 5, 11, 14, 20, and 23** are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent Application Publication 20030231625 to Calvignac et al in view of U.S. Patent 6,393,026 to Irwin and in further view of U.S. Patent 7,197,035 to Asano.

The combination of Calvignac and Irwin discloses the limitations of parent claims 1, 10, and 19. However, combination of Calvignac and Irwin does not disclose expressly the limitations of dependent claims 2, 5, 11, 14, 20, and 23.

Regarding claims 5, 14, and 23, Asano discloses said security and classification functions comprise performing a Network Address Translation (NAT) function to provide subnet independence throughout. Consider, for example, lines 34-41 of column 3 which describes an

efficient NAT function as an object of Asano's inventions. Further, the Asano discloses the limitations of claims 2, 11, and 20 that the security and classification functions comprise replacing a source address associated with header information of a first data packet with an address selected from a pool of router addresses associated with said router in lines 27-35 of column 11 as well as lines 20-33 of column 12. These passages explain that the local source addresses of computers 12-x are replaced by a global address of the router and that this global address is selected from a pool of IP addresses. Calivgnac, Irwin, and Asano are analogous art because they are from the same field of endeavor of high-speed packet processing.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to explicitly add well known network address translation (NAT) functionality to the combination of Calivgnac and Irwin. The motivation for doing so would have been help solve the problem of a shortage of 32-bit IP addresses as suggested by Asano in lines 18-30 of column 1. Therefore, it would have been obvious to combine Asano with Calivgnac and Irwin for the benefit of helping solve the shortage of 32-bit IP addresses to obtain the invention as specified in claims 2, 5, 11, 14, 20, and 23.

11. Claims **3, 4, 12, 13, 21, and 22** are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent Application Publication 20030231625 to Calvignac et al in view of U.S. Patent 6,393,026 to Irwin and in further view of U.S. Patent Application Publication 2004/0100956 to Watanabe.

The combination of Calvignac and Irwin discloses the limitations of parent claims 1, 10, and 19. However, combination of Calvignac and Irwin does not disclose expressly the limitations of dependent claims 3, 4, 12, 13, 21, and 22.

Regarding claims **3, 12, and 21**, Watanabe discloses the limitation that said security and classification functions comprise filtering a first data packet based on at least one of: I) a Layer 2 address associated with said first data packet; 2) a Layer 3 address associated with said first data packet; and 3) a traffic type associated with said first data packet in paragraphs 44 and 45 of page 3 which describe layer 3 addresses (IP addresses) and traffic types (service type) as areas of the header that are used by the search tree for filtering packets. Further, regarding claims **4, 13, and 22**, Watanabe discloses the limitation that said security and classification functions comprise filtering a first data packet based on at least one of: i) a Layer 4 address associated with said first data packet; and 2) a class of service (COS) value associated with said first data packet in paragraphs 52-54 of page 3 which indicates that layer 4 addresses (TCP and UDP ports) can also be used to filter the packets. Calvignac, Irwin and Watanabe are analogous art because they are from the same field of endeavor of high speed packet processing.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to add the packet filtering means of Watanabe to the combination of Calvignac and Irwin. The motivation for doing so would have been to improve the security of the network served by the router by implementing functionality such as a firewall. This is suggested by Watanabe in paragraph 4 and 10 on page 1. Therefore, it would have been obvious to combine Watanabe with the combination of Calvignac and Irwin for the benefit of improved security to obtain the invention as specified in claims 3, 4, 12, 13, 21, and 22.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

- U.S. Patent Application Publication 2004/0078485 to Narayanan discloses a method for providing automatic ingress filtering.
- U.S. Patent 7,200,144 to Terrell, et al discloses a router using network addresses for virtualization.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Robert C. Scheibel whose telephone number is 571-272-3169. The examiner can normally be reached on Mon and Thurs (6:30-5:00) and Fri (6:30-12:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wing F. Chan can be reached on 571-272-7493. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

RCS 11-15-07

Robert C. Scheibel
Patent Examiner
Art Unit 2619

11/19/07

WING CHAN
SUPERVISORY PATENT EXAMINER